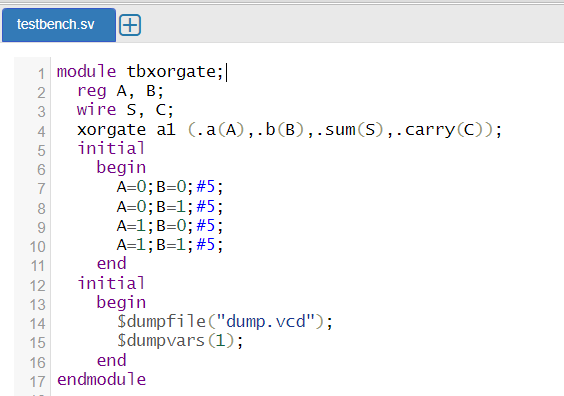
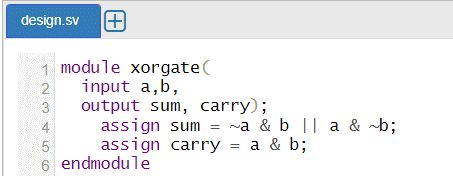
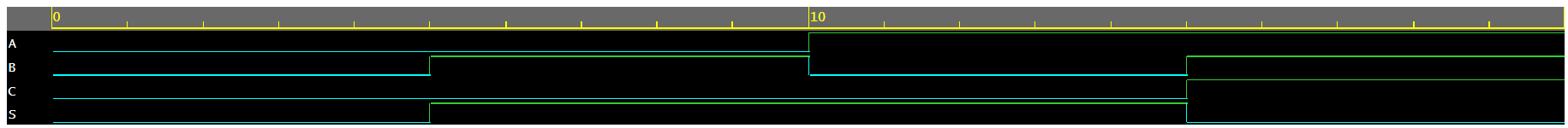
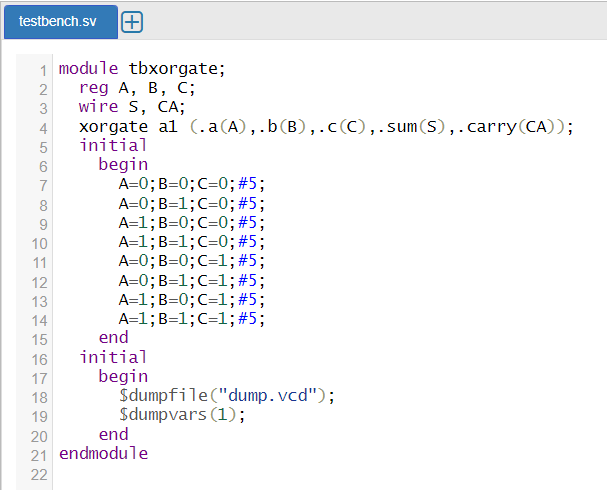
**Lab 4: Design Half Adder & Full Adder Using Half Adder**

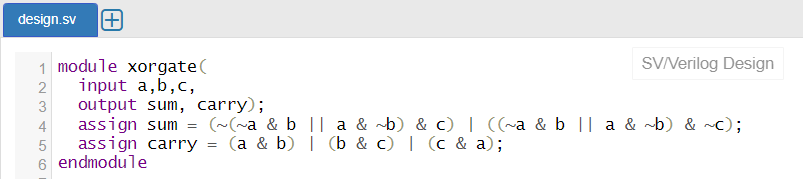
**Question 1: Write Verilog code for half adder. Test using waveform**

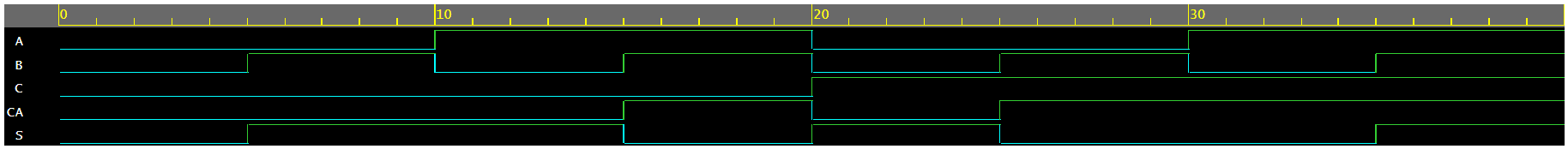
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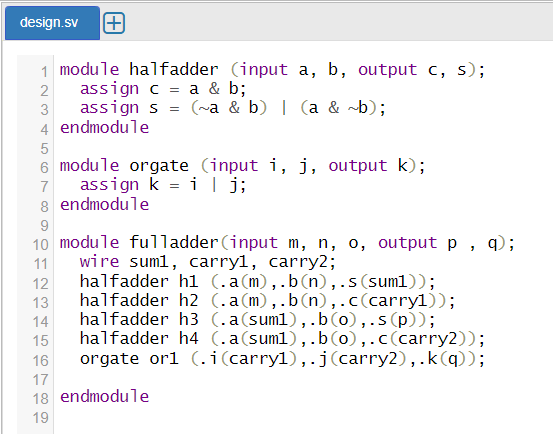
**Question 3. Write Verilog code for full adder. Test using waveform.**

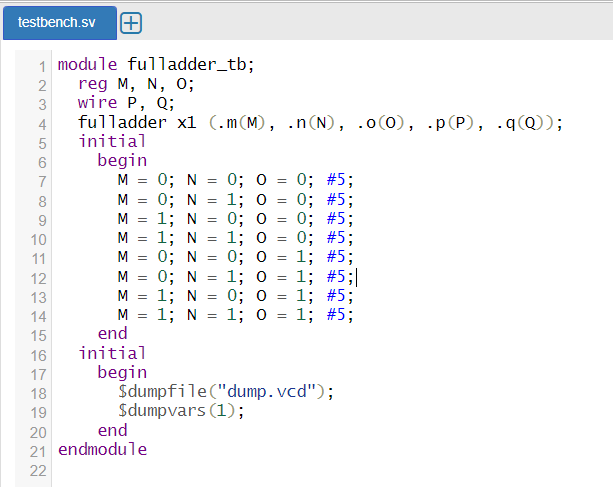
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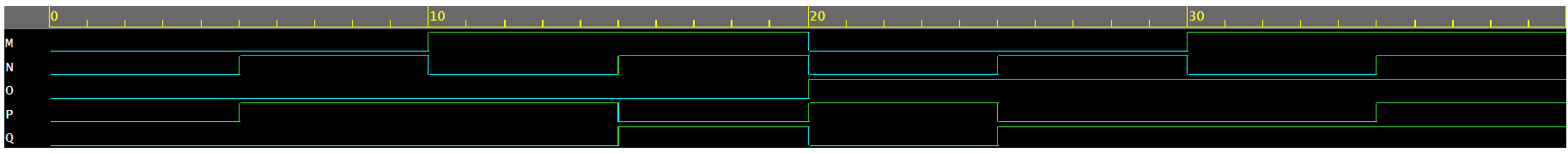
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**Question 4. Write Verilog code for full adder using module instantiation of half adder. Test using waveform.**

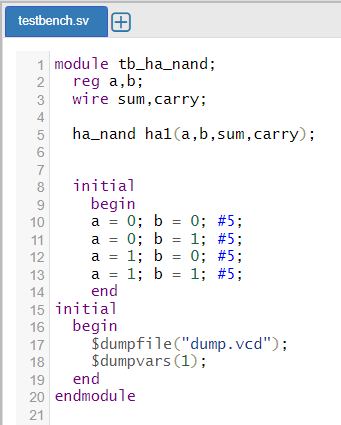
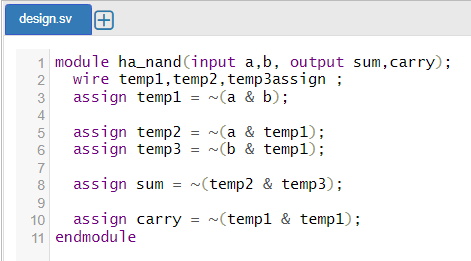
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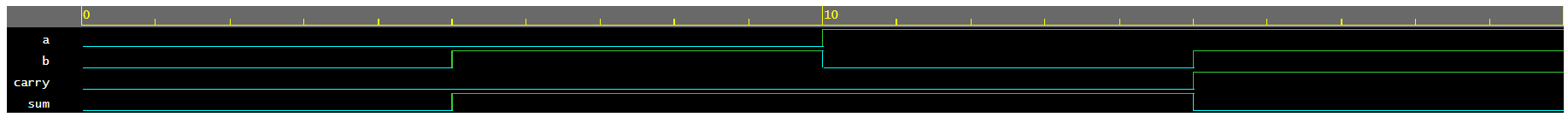
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**Question 5. Write Verilog code for half adder using only NAND gate. Test using waveform**



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